102(e). No new matter has been entered. Claims 1-11 and 19-29 are presented for consideration.

Claim Objections

Claim 23 was objected to for formal matters. Claim 23 has been amended as suggested in the Office Action. Accordingly, Applicants request reconsideration and withdrawal of the objection to claim 23.

35 U.S.C. § 102(e)

Claims 1-11 and 19-27 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wert (U.S. Patent No. 6,281,706). In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention. Applicants respectfully request reconsideration of this rejection.

Claim 1 recites a method of controlling an output buffer circuit for generating an output signal and outputting the output signal from an output terminal. The output buffer circuit includes a first drive circuit for receiving an input signal and a second drive circuit connected to the output terminal and having a lower impedance than the first drive circuit. The method includes generating a first output signal having a first state in accordance with the input signal using the first drive circuit. The second drive circuit is driven to generate a second output signal having the first state by a driving signal which is generated by adding a predetermined delay to the output signal.

Claim 5 recites an output buffer circuit. This circuit includes a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first

output signal having a first state. A second drive circuit is connected to the output terminal and has a lower output impedance than the first drive circuit. The second drive circuit generates a second output signal. A first control circuit is connected to the second drive circuit for generating a first control signal for driving the second drive circuit on the basis of the input signal and a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state.

Accordingly, the second output circuit of the present invention is controlled to generate a signal having a level that is the same as the first drive circuit output signal.

Wert is directed to a boost circuit including a first drive circuit (701, 711), a second drive circuit (705, 717), and two inverters (707, 709). The second drive circuit (705, 717) of Wert is driven by a delay signal generated by delaying a booster output signal using inverter (728) (shown in Figure 7A). The second drive circuit, however, generates an output signal that has a level that is different from that of the first drive circuit (701, 711) in response to the delay signal.

In contrast, the second drive circuit of the present invention is controlled to generate a signal having a level that is the same as that of the first drive circuit output signal. The difference between Wert and the present invention is based on Wert using the second drive circuit to quickly raise the output signal of the booster. In contrast, the present invention uses the first and second drive circuits to generate an output signal having a gentle wave form.

The difference in the levels in the output signals of the first and second drive circuits of Wert is clearly illustrated in Figure 7B. Curves 742 and 756 illustrate the

output of the first drive circuit. Curves 744 and 754 illustrate the output of the second drive circuit. Curve 740 illustrates the input signal. A comparison of curves 742 and 744 illustrates that the output of the second drive circuit (705, 717) is over twice the output level of the first drive circuit. Similarly, when signal 740 transitions from high to low, the output level of the second drive circuit shown by curve 754 is higher than the output level of the first drive circuit illustrated by curve 756.

Accordingly, Wert fails to teach and/or suggest the recited invention. Specifically, Wert fails to teach and/or suggest driving the second drive circuit to generate a second output signal having the first state by a driving signal which is generated by adding a predetermined delay to the output signal. Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-11 and 19-27 under 35 U.S.C. § 102(e).

New Claims

New claims 28 and 29 are added by the present Amendment to claim additional features of the present invention. For at least the reasons discussed above regarding claims 1-11 and 19-27, claims 28 and 29 are allowable. Accordingly, Applicants respectfully request consideration and allowance of claims 28 and 29.

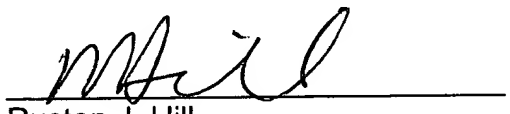
Conclusion

Applicants' amendments and remarks have overcome the objection and rejection set forth in the Office Action dated November 1, 2002. Specifically, Applicants' amendment to claim 23 overcomes the objection to claim 23. Applicants' remarks have

distinguished claims 1-11 and 19-27 from Wert, and thus overcome the rejection of these claims under 35 U.S.C. § 102(e). New claims 28 and 29 have been added to further claim Applicants' invention. Accordingly, claims 1-11 and 19-29 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-11 and 19-29.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 108075-00022.

Respectfully submitted,



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Enclosures: Marked-Up Copy of Amended Claims
Petition for Extension of Time

MARKED-UP COPY OF AMENDED CLAIMS
AS REQUIRED UNDER 37 C.F.R. § 1.121

1. (Twice Amended) A method of controlling an output buffer circuit for generating an output signal and outputting the output signal from an output terminal, wherein the output buffer circuit includes a first drive circuit for receiving an input signal, and a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit; and

driving the second drive circuit to generate a second output signal having the first state [after the first output signal is changed by a predetermined amount by the first drive circuit] by a driving signal which is generated by adding a predetermined delay to the output signal.

2. (Thrice Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit to generate a second output signal having the first state [after the first output signal is changed by a predetermined amount by the first drive circuit] by the control signal.

5. (Thrice Amended) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, wherein the second drive circuit generates a second output signal [having the first state]; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and [the first output signal after the first output signal is changed by a predetermined amount by the first drive circuit] a delay signal which is generated by adding a predetermined delay to the first output signal such that the second drive circuit generates the second output signal having the first state.

23. (Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor of a first type and a second output transistor of a second type, the second drive circuit including a third output transistor of the first type and a fourth output transistor of the

second type, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal by turning on the first transistor of the first drive circuit; and

driving the second drive circuit to [generated] generate a second output signal having the first state by turning on the third transistor of the second drive circuit [after the first output signal is changed by a predetermined amount by the first drive circuit] by a driving signal which is generated by adding a predetermined delay to the first output signal.

25. (Amended) An output buffer circuit comprising:

a first drive circuit including a first transistor of a first type and a second output transistor of a second type which are connected to an output terminal, wherein the first and second transistors receive an input signal and generate a first output signal having a first state by turning on the first transistor or the second transistor;

a second drive circuit including a third transistor of the first type and a fourth transistor of the second type which are connected to the output terminal, wherein the third and fourth output transistors have lower impedances than the first and second output transistors [and generate a second output signal]; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for turning on the third transistor on the basis of the input signal and [the first output signal after the first output signal is changed by a predetermined amount by the first drive circuit] a delay signal which is generated by adding a predetermined delay

to the first output signal such that the second drive circuit generates a second output signal having the first state.